IN THE CLAIMS:

For the convenience of Examiner, the complete listing of claims in the present application is provided below.

1. (Original) A method to design a circuit, the method comprising:

determining first statistical circuit activity data at a plurality of nodes of a first design of the circuit;

transforming a first portion of the first design to generate a second portion of a second design of the circuit;

selectively determining at least one node in the second portion of the second design; and

determining second statistical circuit activity data for the at least one node in the second portion of the second design from the first statistical circuit activity data.

2. (Original) A method as in claim 1, wherein the first portion of the first design includes at least one of the plurality of the nodes of the first design.

3. (Original) A method as in claim 1, wherein the second statistical circuit activity data comprises:

a) probability information of state transition at a node;

b) probability information of the node being at a state; and

c) probability information of a group of nodes being at a state.

4. (Original) A method as in claim 1, wherein a subset of nodes of the plurality of nodes of the first design remain unchanged in the second design after the first portion of the first design is transformed; and, a portion of the first statistical circuit activity data is maintained for the subset of nodes in the second design.

5. (Original) A method as in claim 4, further comprising:

transforming a third portion of the second design to generate a fourth portion of a third design of the circuit;

selectively determining at least one node in the fourth portion of the third design; and

determining third statistical circuit activity data for the at least one node in the fourth portion of the third design from a portion of:

a) the first statistical circuit activity data; and

b) the second statistical circuit activity data.

6. (Original) A method as in claim 5, wherein one or more signals at the at least one node in the second portion of the second design drive the third portion of the second design.

7. (Original) A method as in claim 1, wherein the second statistical circuit activity data is determined from a formal Boolean analysis.

8. (Original) A method as in claim 1, wherein the first design is one of: a) a register transfer level (RTL) design, and b) a behavioral level design; and, the first portion of the first design is transformed to generate a gate level design.

9. (Original) A method as in claim 1, further comprising: